The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ANGELA HUI, SHENQING FANG, HIROYUKI KINOSHITA, KELWIN KO, WENMEI LI, YU SUN, HIROYUKI OGAWA, and CHI CHANG

Appeal No. 2005-0269
Application No. 10/032,757

ON BRIEF

Before HAIRSTON, KRASS, and BARRY, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 2 and 3. Claim 1 has been cancelled, claims 7-15 have been withdrawn, and claims 4-6, and 16-19 have been indicated by the examiner as being directed to allowable subject matter.

The invention is directed to semiconductor devices. In particular, a dual gate structure is formed in a nonvolatile memory using a protective layer.

Independent claim 2 is reproduced as follows:

2. A semiconductor device including a core and a periphery, the semiconductor device comprising:

a plurality of core gate stacks in the core, each of the plurality of core gate stacks including a first polysilicon gate and a Wsi layer above the first polysilicon gate, wherein each of the plurality of core gate stacks includes an edge;

a plurality of core spacers, each of the plurality of core spacers residing along an edge of the plurality core gate stacks;

a plurality of sources in the core, the plurality of sources residing between a portion of the plurality of core gate stacks; and

a plurality of periphery gate stacks in the periphery, each of the plurality of periphery gate stacks including a second polysilicon gate and a CoSi layer on the second polysilicon gate.

The examiner relies on the following reference:

Lien	6,338,993	Jan. 15, 2002 (filed Aug. 18, 1999)

Claims 2 and 3 stand rejected under 35 U.S.C. § 102(e) as anticipated by Lien.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

A claim is anticipated only when a single prior art reference expressly or inherently discloses each and every element or step thereof. Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 1570, 1569, 7 USPQ2d 1057, 1064 (Fed. Cir. 1988); RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984). If the examiner presents a reasonable basis for alleging inherency, the burden shifts to appellants to come forward, if they can, with evidence to the contrary. In re King, 801 F.2d 1324, 1327, 231 USPQ 136, 138-39 (Fed. Cir. 1986); In re Ludtke, 441 F.2d 660, 662, 169 USPQ 563, 565 (CCPA 1971); In re Swinehart, 439 F.2d 210, 213, 169 USPQ 226, 229 (CCPA 1971).

At pages 5-6 of the answer, the examiner applies the teachings and elements of Lien to each and every claimed limitation, indicating exactly how Lien anticipates the instant claimed subject matter. We have reviewed the examiner's reasoning, the Lien patent disclosure, and the instant claims and we find the examiner's rationale to be sound. In view of this prima facie case of anticipation, the burden shifted to appellants to come forward with evidence to the contrary.

Appellants' sole argument is to contend that Lien does not disclose a "plurality of core spacers, each of the plurality of core spacers residing along an edge of the plurality of core gate stacks" (principal brief, page 4). In particular, appellants take issue with the examiner's identification of Lien's element 400 to show the claimed spacers because element 400 is a protective silicon nitride layer deposited over memory cell region 30, NMOS region 20, and PMOS region 10.

It is clear from Lien, that the silicon nitride layer 400 is further processed to develop "spacers" 410 and 420, shown in Figure 7, and that elements 410 and 420 are even identified in Lien as "spacers" (see, for example, column 4, lines 2 and 17). While not described as such, it is also clear, from the right side of Figure 7 of Lien, that layer 400 does form a "spacer" between core stacks.

Appellants admit that the layer 400 is formed into spacers (principal brief, page 5) but contend that the spacers are formed in the peripheral logic region, rather than the memory cell region (principal brief, page 5). Claims 2 and 3 do not recite a "memory cell region," but, assuming that appellants refer to the claimed "core" as denoting the memory cell region, and "periphery" as denoting the peripheral logic region, layer 400 in

Lien forms spacers along the edge of the plurality of the core gate stacks on the right side of Figure 7, as per instant claim 2, while spacers 410 and 420 reside along the edges of the periphery gate stacks on the left side of Figure 7, as per instant claim 3.

Appellants assert, at page 3 of the reply brief, that since Lien's nitride spacers 420 are formed by etching the silicon nitride layer 400, spacers are formed only by etching and, since layer 400 is not etched, it cannot qualify as a spacer, as claimed. We disagree. While it is true that spacers 410 and 420 of Lien are formed by etching, we find nothing in the broad language of the instant claims which precludes layer 400 of Lien from also being a spacer, since layer 400 clearly lies on the edge of the core gate stacks and acts as "spacers" to the same extent as spacers 410 and 420 of Lien and/or to the same extent as the spacers recited in instant claims 2 and 3.

The examiner's decision rejecting claims 2 and 3 under 35 U.S.C. § 102(e) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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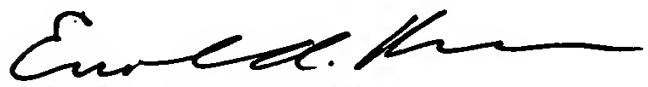
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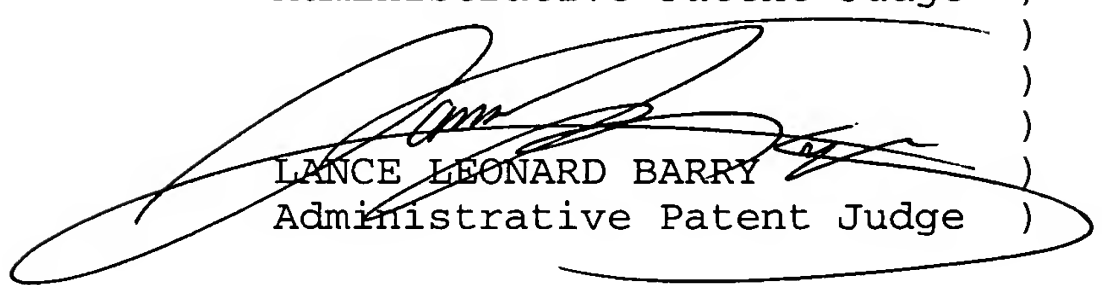
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LANCE LEONARD BARRY)
Administrative Patent Judge)

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